technique, such that it contacts top surface of the GaAs wafer between the source layers and the drain and so supports both sides of the wafer over the air layer of the drain, whereby a gate having π – structure results.] comprising:

a substrate having top and bottom surfaces;

first and second source layers over the top surface of the substrate;

a GND layer formed on the bottom surface of the substrate and grounded to the first and second source layers by way of a back-side via-hole process;

a drain formed on the top surface of the substrate between the first and second source layers;

an air layer formed over the drain;

first and second gate footsteps formed between the first and second source layers and the drain; and

a metal layer having a π structure formed using an air bridge technique over the top surface of the substrate so as to contact the substrate at the first and second gate footsteps between the first and second source layers and the drain, thereby forming a gate and laterally supporting opposite ends of the substrate over the air layer.

Clean Amended Claim:

1. (Amended) A transistor comprising:

a substrate having top and bottom surfaces;

first and second source layers over the top surface of the substrate;

a GND layer formed on the bottom surface of the substrate and grounded to the first and second source layers by way of a back-side via-hole process;

a drain formed on the top surface of the substrate between the first and second source layers;

an air layer formed over the drain;

first and second gate footsteps formed between the first and second source layers and the drain; and

a metal layer having a π structure formed using an air bridge technique over the top surface of the substrate so as to contact the substrate at the first and second gate footsteps between the first and second source layers and the drain, thereby forming a gate and laterally supporting opposite ends of the substrate over the air layer.

New claims:

3. (New) The transistor of claim 1, wherein the substrate comprises gallium arsenide.

4. (New) The transistor of claim 1, wherein the air layer is formed over the drain by means of acetone lifting-off of the metal layer.

5. (New) The transistor of claim 1, wherein the metal layer is formed by way of vapor deposition.

6. (New) The transistor of claim 1, wherein the metal layer comprises Ti/Au.